Patent Claims

1. An arrangement for a junction between a microstripline and a waveguide, comprising

- a microstripline (ML) which is fitted on the upper face of a dielectric substrate (S),
- a waveguide which is fitted on the upper face of the substrate (S) and has an opening (OB) on at least one end surface and has a structure (ST) which is in the form of a step or steps in the area of the opening (OB) on one side wall and is conductively connected in at least one part (ST1) to the microstripline (ML), and wherein one side wall of the waveguide is a metallized layer (LS) formed on the substrate (S),
- a cutout (A) which is formed in the metallized layer (LS) and into which the microstripline (ML) projects,
- rear-face metallization (RM) which is formed on the rear face of the substrate (S), and
- electrically conductive via holes (VH) between the metallized layer (LS) on the upper face of the substrate (S) and the rear-face metallization (RM), which surround the cutout (A).

2. The arrangement as claimed in claim 1, **characterized in that** the waveguide (B) is a surface mounted device.

3. The arrangement as claimed in claim 1 or 2, **characterized in that** the structure (ST) which is in the form of a step or steps is formed on that side wall of the waveguide (B) which is opposite the cutout (A).

4. The arrangement as claimed in one of the preceding claims, **characterized in that** the distance between the via holes (VH) is chosen such that the radiated emission of the electromagnetic wave in the useful frequency range through the intermediate spaces is

small, and the operation of the junction is thus not adversely affected by increased losses or undesirable couplings.

5. The arrangement as claimed in claim 4, **characterized in that** the via holes (VH) run in a number of rows which are arranged parallel to one another.

6. The arrangement as claimed in one of the preceding claims, **characterized in that** the substrate (S) has a waveguide opening (DB) in the area of the metallized layer (LS) on the upper face of the substrate (S).

7. The arrangement as claimed in claim 5, **characterized in that** the inner surface of the waveguide opening (DB) is electrically conductive.

8. The arrangement as claimed in claim 5 or 6, **characterized in that** that side wall of the waveguide (B) which is opposite the upper face of the substrate has a structure (ST), which is in the form of a step or steps, in the area of the waveguide opening (DB).